

MMT-188EB

80C188EB Microprocessor Board
Rev H

HARDWARE / SOFTWARE
USER'S REFERENCE MANUAL
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PREFACE

User Feedback

At Midwest Micro-Tek we are always interested in user comments and suggestions. We would like to know how well you like our products. We also like to know if you feel there is something missing either in terms of features offered, or in our documentation. We value your ideas and information!

Customization

Midwest Micro-Tek will modify hardware and software to customer specifications with a minimum quantity purchase, or on a consulting basis.

PRIOR TO INSTALLATION

- ! Set the necessary jumpers on the MMT-188EB board for the memory and I/O configuration intended. See Section 2-5, Memory Configuration on pages 9-11.

- ! Verify that the terminal cable you are using is correct as specified in Appendix B of this manual. It may be necessary to jumper the CTS (clear to send) signal on the board for communication with your terminal device. The MMT-188EB is configured as a DCE device and may require a NULL modem connector to communicate with older PC's. Please check your PC specifications for RS-232 compatibility.

- ! Midwest Micro-Tek cannot assume responsibility for problems caused by improper power supply connections.

- ! Before operating the MMT-188EB embedded controller, please verify that the +5 volt power supply is plugged into a wall socket, and the power lead is connected to the controller's power jack

PREFACE

Supplemental Materials

This manual provides general information, installation instructions, programming specifications, principles of operation, and service information for the MMT-188EB microcomputer board.

Supplemental information may be found in the data sheets included on the CD-ROM. The following data sheets are included on the CD-ROM:

!	80C188EB.PDF	<u>Intel 80C186EB / 80C188EB User's Manual</u>
!	82C55.PDF	<u>Programmable Peripheral Interface</u>
!	MAX690A.PDF	<u>Maxim Microprocessor Supervisory Circuit</u>
!	DS1315.PDF	<u>Dallas Semiconductor Phantom Time Chip</u>
!	24LC16B.PDF	<u>16K Serial EEPROM</u>
!	AM29F016.PDF	<u>AMD 2MB Flash Memory</u>
!	MAX197.PDF	<u>Maxim 12-Bit D/A Converter</u>
!	MAX527.PDF	<u>Maxim 12-Bit A/D Converter</u>

The above references give excellent information for the complete utilization of the MMT-188EB microcomputer board. It is beyond the scope of this document to instruct the user in assembly language, or higher level language programming.

User Assistance

If the information you need for configuring this board is not present in this document, please do not hesitate to call us for technical support. At Midwest Micro-Tek, we want to make the use of this board as pleasant and trouble free as possible.

PREFACE

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CHAPTER ONE - Specifications

1-1 Introduction

Thank you for purchasing the MMT-188EB. We hope that you find it to be reliable, flexible and easy to use. This board is a complete microcomputer, requiring only a +5 volt power supply to operate.

This board has received a 50 hour dynamic burn-in under continuous loop diagnostics to insure a high level of reliability for your product.

Manual Notation

Every discussion of microprocessor systems requires a method of denoting an active low signal. This manual uses a "#" pound symbol following the label name to indicate such signals. Additionally, when referring to bits within a byte, the 8 bits are assumed to be numbered 0 through 7 with 0 being the least significant of these. Lastly, the designation of "HIGH" and logic level "1" is equivalent to a bit being set and "LOW" or "0" as a bit being cleared. These are used throughout this manual. All notations used in this manual are consistent with the notations used by major IC industry sources.

The notation used in the jumper tables in this document are as follows:

1&2	A 3-pin block with a jumper installed on pins 1 and 2
2&3	A 3-pin block with a jumper installed on pins 2 and 3
ON	A 2-pin block with a jumper installed
OUT	No jumper installed on this block
XXX	Does not matter

1-2 General Description

Standard Features

- ! Intel 80C188EB CPU at 20 MHz
- ! Up to 1 MB of fully addressable memory
- ! 2 Serial I/O ports (2 - RS-232 standard or 2-RS-422/485 optional)
- ! 24 bits of parallel I/O
- ! 2 counter/timers
- ! 3 Hardware Interrupt Lines
- ! Watchdog timer & Power fail detector
- ! 60-pin header for direct access to uP and peripheral lines
- ! 3 Status LEDs

Options

- ! 8 channels of 12-bit analog to digital converter
- ! 4 channels of 12-bit digital to analog converter
- ! Dallas Semiconductor Phantom Time Chip and nonvolatile memory controller
- ! RS-485 Line Driver/Receiver for Serial Communications
- ! 8-Pin DIP Switch for LAN Operation
- ! Monitor/Debugger EPROM and 32kx8 SRAM
- ! EPROM & SRAM
- ! Parallel, Serial, and Power Cabling
- ! Interface for an LCD and a 4x4 keypad
- ! 2 MB Flash
- ! ROMDOS on EPROM with a 2MB Flash Disk

1-3 Equipment Supplied

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- ! MMT-188EB Microcomputer Board
- ! CD-ROM containing:
 - " I/O Equates
 - " Sample Code
 - " Manuals
 - " Datasheets
 - " Schematics
 - " Silk Screen

1-4 Equipment Required

- ! +5 volt DC power supply - 1A minimum
- ! Serial I/O terminal or PC with communication software (Procomm or HyperTerminal is suggested)

1-5 Specifications

Standard Features

- ! Intel 80C188EB microprocessor
 - " 20 MHz CPU clock rate
 - " Operating Temperature range: -40 EC to 85 EC
 - " RH: to 90% without condensation
- ! Up to 1 MB of fully addressable memory in the form of
 - " 2 32-pin "byte-wide" memory sockets which may contain up to 2, 512kx8 bit memory units for a possible 1 MB of memory
 - " Up to 512kx8 RAM / ROM / EPROM / EEPROM / 5V FLASH (32 pin socket U3)
 - " Up to 512kx8 SRAM (32 pin socket U4)
- ! 2 Serial I/O ports
 - " Asynchronous rates to 115K baud
 - " Synchronous rates to 4 Mbaud
 - " RS-232 interface
 - " RS-485 interface (optional)
 - Party Line or point-to-point
 - Communication distances up to 5000 feet
 - " RTS and CTS for handshaking
- ! 24 bits of parallel I/O
 - " 24 bits of parallel I/O via Intel 82C55A (or compatible)
 - Terminated at an OPTO22 Standard 50-pin straight header
- ! 2 counter/timers available to the user
- ! Watchdog Timer & Power Fail Detector

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- ! 60-pin header
 - " Access to all data and address lines
 - " Clock output at 1/2 the oscillator frequency
 - " Read and Write Lines (RD# and WR#)
 - " 2 timer/counters
 - " +5 and ground
 - " 3 User I/O chip selects
 - " Off-board memory chip selects
 - " Nonmaskable interrupt
 - " 2 Maskable interrupts
 - " Reset (Output)
 - " Ready (Input)
 - " Hold and Hold Acknowledge
 - " Battery Voltage (Input/Output)

Options

- ! 8 channels of 12-bit analog to digital converter
- ! 4 channels of 12-bit digital to analog converter
- ! Dallas Semiconductor Phantom Time Chip and nonvolatile memory controller
- ! RS-485 Line Driver/Receiver for Serial Communications
- ! 8-Pin DIP Switch for LAN Operation
- ! Monitor/Debugger EPROM and 32kx8 SRAM
- ! EPROM & SRAM
- ! Parallel, Serial, and Power Cabling
- ! 2 MB Flash
- ! ROMDOS on EPROM with a 2MB Flash Disk

CHAPTER TWO - Getting Started

2-1 Installation Considerations

The MMT-188EB microcomputer board is designed as a stand-alone single board computer (SBC). A Monitor/Debugger EPROM and 8kx8 SRAM are available as an option to allow the user to start exercising the board immediately.

The MMT-188EB is shipped without memory devices installed in the 32-pin "byte wide" sockets. However, a Monitor /Debugger EPROM and SRAM can be installed at an additional cost.

Note: It is important that the user's startup code reside in memory socket U3 due to the characteristics of the chip select UCS#.

2-2 Static Electricity (ESD) Considerations

Memory devices are extremely sensitive to static electricity. When installing memory devices, be sure that the power to the board is off and pin 1 of the device is properly oriented. A grounded, static-dissipating wrist strap should also be used in order to minimize possible static damage.

2-3 Jumper Installation

The MMT-188EB CPU board has been designed to be extremely flexible in allowing the user to configure memory and I/O as needed for his/her particular product needs. A wide variety of "byte-wide" parts may be used in memory sockets U3 and U4.

As shipped, the board has jumpers installed for the following configuration:

Jumper	Pins Jumped	Usage
JP3	2&3	32kx8 EPROM installed in location U3
JP4	1&2	32kx8 RAM installed in location U4
JP5	1&2	32kx8 EPROM installed in location U3
JP9	2&3	32kx8 RAM installed in location U4
JP10	2&3	32kx8 EPROM installed in location U3
JP11	1&2	32kx8 EPROM installed in location U3
JP24	1&2	32kx8 EPROM installed in location U3
JP14	1&2	CTS0# grounded for 'always on' reception of characters
JP15	2&3	RS-232 interface enabled
JP16	1&2	CTS1# grounded for 'always on' reception of characters
JP17	2&3	RS-232 interface enabled

Refer to silkscreen for location of memory IC's U3 and U4 and jumper blocks. Additional detailed sections are provided describing each of these options. Refer to Section 2-5: Memory Configuration & Appendix A - Jumper Settings.

CHAPTER TWO - Getting Started

2-4 Serial I/O

The two DCE serial interfaces of the MMT-188EB board are configured as 9 pin serial interface connectors compatible in pin numbering with the IBM PC 9 pin serial I/O connectors. Both serial connectors are presented to the outside world via 10-pin headers, which can be transformed into DB9 socket connectors by way of ribbon cables. Please refer to Appendix B for proper pinouts of the 10-pin stake headers.

Two electrical interface specifications have been provided by MMT on the MMT-188EB board. Both RS-232 and RS-485 are available. RS-232 is the "standard" interface used by most computer users and will be the interface of choice for most installations. Both serial connections can be configured as independent RS-232 ports. Cabling distances of up to 50 feet are possible at 9600 baud, with longer distances possible as the baud rate is decreased. RS-485 is provided as an option for both serial channels. The 485 interface can operate reliably at up to 5000 feet. This interface can be configured to operate in a "party line" mode with multiple "drops" along its entire length.

The jumper configuration for these modes is outlined in Appendix A. All MMT boards are shipped with serial ports configured as RS-232 devices. Serial channel 0 is the default channel for the connection of the host PC. Connect this channel to the PC's COM port if the MMT Monitor/Debugger is in use.

Refer to the silkscreen for location of the 10-pin stake headers and jumper blocks. J2 is channel 0 and J1 is channel 1.

RTS and CTS Considerations

Each RTS_x# (x = 0-1) (Request to Send) signal is controlled by toggling a parallel I/O bit directly in the 80C188EB. The 80C188EB is equipped with 16 latched bits of parallel I/O. However, most of these bits are multiplexed with other control signals, so they cannot be used for data transfer.

The RTS_x# control signals have two basic functions. When using the RS-232 interface, RTS_x# is used as a handshaking signal to drive pin 8 of the DB9 socket connectors. During RS-485 operation, RTS_x# is used to control whether the 75176 Line Driver IC is transmitting or receiving. When RTS_x# is cleared, the 75176 receives data from the serial port. When this bit is set, the 75176 transmits data to the serial port.

Note: When using the RS-232 or RS-485 interface, the RTS₀# and RTS₁# lines are not automatically toggled. The user must output the correct word to the P2PIN register of the 80C188EB to set or reset these signals.

The CTS_x# inputs on the 80C188EB are used as handshaking signals to control the data flow on the serial I/O channels. When CTS_x# is tied directly to ground, the serial channel is in "receive always" mode.

The CTS_x# signals can be tied directly to ground (default setting) with jumpers JP14 & 16, or sent out to the DB9 socket connections to be driven by other I/O devices.

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JP14 (Ch 0) & JP16 (Ch 1) - Description

The CTSx# (Clear to Send Serial Port x) if installed on pins 2&3, this jumper allows pin 7 of the DB9 socket connector to drive the CTSx line of the Serial Port x interface. On pins 1&2, the jumper forces the serial channel into the "always on" mode.

RS-485 Operation

RS-485 interface allows the separation of the MMT-188EB and peripherals up to 5000 feet. A 75176 IC is used to accomplish this by using a differential pair. Please note that a full duplex configuration is not possible and the device desiring to transmit must raise the direction control line of the 75176 (RTSx signals are used for this toggle). A Master/Slave relationship under software control is generally the most straight forward communications scheme to implement. Optional LAN circuitry is available which provides a method of addressing up to 256 slave MMT-188EBs.

Networking using RS-845

Various RS-485 configurations:

1. Interfacing one SBC to a PC using a serial link:

! To use only one SBC interfaced to a PC, one needs to set up the SBC using the 75176 setup on the far left of Figure 2-4.1. In doing so, enable the 100 ohm and both the 560 (or 1K) ohm resistors. Next determine if both the PC and SBC are connected to a common earth ground. If this is not the case, enable the 100 ohm resistor and add a grounding wire to your twisted pair. The 100 ohm resistor insures that a damaging current build up between the two ports is prevented. Refer to tables 2-4.1 and 2-4.2 for the biasing and grounding jumper settings.

2. Interfacing two SBC's together:

! To interface two SBC's, refer to the two outer 75176 configurations on Figure 2-4.1. Configure the first (master) board as described in Part 1 of this page and configure the second (slave) board by enabling the 100 ohm biasing resistor. Refer to tables 2-4.1 and 2-4.2 for the biasing and grounding jumper settings. Again, if a common ground is not present, enable the grounding resistor on each board and add a grounding wire to the twisted pair.

3. Interfacing more than two SBC's:

! When interfacing more than two SBC's, refer to the entire Figure 2-4.1. As shown, as many as 32 nodes can be added in line with the twisted pair. Note that any board that is added to the network should not have any of the biasing resistors enabled since the master board is performing the biasing for the entire network. The only boards that need the biasing resistors enabled is the master (first terminal node) and the last board (final terminal node). Refer to tables 2-4.1 and 2-4.2 for the biasing and grounding jumper settings. If one or two or any number of the boards do not share a common earth ground, one must enable the grounding resistor and add a grounding wire to the twisted pair.

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Configuration	JP15	JP29	JP26	JP28	JP25
Master	1&2	ON	ON	ON	*
Final Node	1&2	ON	OUT	OUT	*
Additional Nodes	1&2	OUT	OUT	OUT	*
RS-232 Operation	2&3	XXX	XXX	XXX	ON

Table 2-4.1: Channel 0 biasing and grounding jumper table

Configuration	JP17	JP27	JP30	JP31	JP37
Master	1&2	ON	ON	ON	*
Final Node	1&2	ON	OUT	OUT	*
Additional Nodes	1&2	OUT	OUT	OUT	*
RS-232 Operation	2&3	XXX	XXX	XXX	ON

Table 2-4.2: Channel 1 biasing and grounding jumper table

- * This is the grounding resistor jumper. To enable it, **DO NOT** place a jumper on the block. To disable it, place a shorting jumper on the block. Refer to instructions in this section for use. (Please note that a jumper must ALWAYS be placed on this block when in the RS-232 mode).

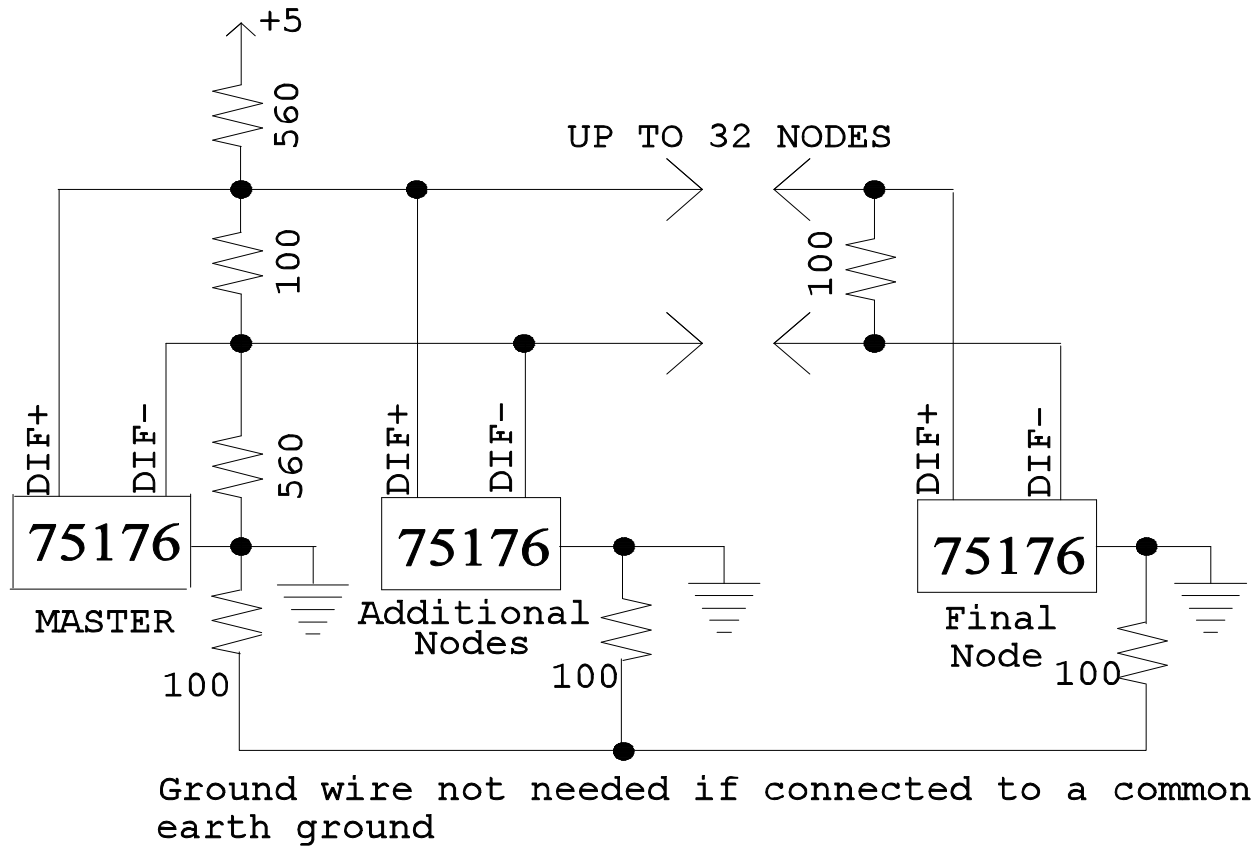


Figure 2-4.1: RS-485 Network Schematic

Serial Channel Interrupts

Transmit and receive interrupts are available on both serial channels. Channel 0 has an interrupt vector associated with both the receive and transmit interrupts: Type 020 and 021 respectively in the 80C188EB interrupt vector table. Serial channel 1 does not have a built in interrupt, but is connected directly to the 80C188EB's INT1 line. This allows both channels to be operated in either the polled, or interrupt driven modes.

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2-5 Memory Configuration

The "byte-wide" sockets of the MMT-188EB board have been configured to be extremely flexible. The following list outlines the types of memory supported.

U3

8kx8, 16kx8, 32kx8, 64kx8, 128kx8, 256kx8, 512kx8 ROM devices
 8kx8, 32kx8, 128kx8, 256kx8, 512kx8 RAM type devices
 32kx8, 64kx8, 128kx8, 256kx8, 512kx8 5V Flash devices
 8kx8, 32kx8, 128kx8, 512kx8 EEPROM type devices

U4

8kx8, 32kx8, 128kx8, 256kx8, 512kx8 RAM type devices

If you have additional "byte-wide" devices to install which are not listed above, please compare to pinout requirements of the devices you wish to install against the possible pin configurations available through the MMT-188EB memory jumper block. The MMT-188EB memory sockets are fully compatible with memory devices from Benchmarq™ and Intel™. Although most manufacturers conform to these specifications, some do not. If you have difficulties with your SBC please verify that your memory is properly installed and follows the specifications above.

JUMPER	8kx8 SRAM	32kx8 SRAM	128kx8 SRAM	256kx8 SRAM	512kx8 SRAM
JP4	2&3	1&2	1&2	1&2	1&2
JP9	2&3	2&3	2&3	1&2	1&2

Table 2-5.1 - RAM Jumpers. RAM Socket U4

JUMPER	8kx8 EPROM	16kx8 EPROM	32kx8 EPROM	64kx8 EPROM	128kx8 EPROM	256kx8 EPROM	512kx8 EPROM
JP3	2&3	2&3	2&3	2&3	1&2	1&2	1&2
JP5	2&3	2&3	1&2	1&2	1&2	1&2	1&2
JP6	OUT	OUT	OUT	OUT	OUT	OUT	OUT
JP7	OUT	OUT	OUT	OUT	2&3	2&3	1&2
JP8	OUT	OUT	OUT	OUT	1&2	1&2	1&2
JP10	2&3	2&3	2&3	1&2	1&2	1&2	1&2
JP11	OUT	1&2	1&2	1&2	1&2	1&2	1&2
JP12	OUT	OUT	OUT	OUT	OUT	OUT	OUT
JP13	OUT	OUT	OUT	OUT	OUT	OUT	OUT
JP24	2&3	2&3	2&3	2&3	2&3	2&3	2&3

Table 2-5.2 - ROM Jumpers. ROM Socket U3

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JUMPER	ATMEL 32kx8 FLASH	Other 32kx8 FLASH	64kx8 FLASH	128kx8 FLASH	256kx8 FLASH	512kx8 FLASH
JP3	2&3	1&2	1&2	1&2	1&2	1&2
JP5	1&2	1&2	1&2	1&2	1&2	1&2
JP6	2&3	OUT	OUT	OUT	OUT	OUT
JP7	OUT	OUT	OUT	OUT	OUT	OUT
JP8	OUT	2&3	2&3	2&3	2&3	2&3
JP10	OUT	1&2	1&2	1&2	1&2	1&2
JP11	1&2	1&2	1&2	1&2	1&2	1&2
JP12	OUT	OUT	OUT	OUT	OUT	OUT
JP13	OUT	2&3	2&3	2&3	2&3	2&3
JP24	2&3	2&3	2&3	2&3	2&3	2&3

Table 2-5.3 - ROM Jumpers. ROM Socket U3 (With FLASH installed)

JUMPER	8kx8 EEPROM	32kx8 EEPROM	128kx8 EEPROM	512kx8 EEPROM
JP3	2&3	2&3	1&2	1&2
JP5	OUT	OUT	1&2	1&2
JP6	OUT	1&2	OUT	OUT
JP7	OUT	OUT	OUT	OUT
JP8	OUT	OUT	OUT	1&2
JP10	OUT	OUT	1&2	1&2
JP11	OUT	1&2	1&2	1&2
JP12	ON	ON	OUT	OUT
JP13	OUT	OUT	2&3	2&3
JP24	2&3	2&3	1&2	1&2

Table 2-5.4 - ROM Jumpers. ROM Socket U3 (With EEPROM installed)

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JUMPER	8kx8 SRAM	32kx8 SRAM	128kx8 SRAM	256kx8 SRAM	512kx8 SRAM	
JP3	2&3	2&3	2&3	1&2	1&2	
JP5	OUT	OUT	OUT	OUT	OUT	
JP6	OUT	1&2	1&2	1&2	1&2	
JP7	OUT	OUT	OUT	OUT	OUT	
JP8	OUT	OUT	OUT	OUT	1&2	
JP10	OUT	OUT	OUT	OUT	OUT	
JP11	2&3	1&2	1&2	1&2	1&2	
JP12	ON	ON	ON	ON	ON	
JP13	OUT	OUT	1&2	1&2	1&2	
JP24	1&2	1&2	1&2	1&2	1&2	RAM tied to +5
	2&3	2&3	2&3	2&3	2&3	RAM tied to battery backup

Table 2-5.5 - ROM Jumpers. ROM Socket U3 (with RAM installed)

2-6 Parallel Port

The MMT-188EB makes use of an Intel 82C55A (or compatible) programmable peripheral interface IC to provide 24 lines of parallel I/O. The 82C55A divides each set of 24 lines into three ports (A, B, and C) of eight lines each. In addition, port C is divided into two groups of four lines each. The 82C55A is software programmable for three modes of operation. Each mode can be configured for various types of I/O formats.

The MMT-188EB's 82C55A IC is terminated into an OPTO22 compatible 50-pin header. Note: A relay is NOT provided to control the state of pin 49 of the OPTO header. Instead, pin 49 is used to supply +5V to the 50-pin header.

The 82C55A resides in I/O space and is selected through GCS5# at the following address:

```
OPTO22          CS_8255# .....          040h - 043h
```

Header pinouts are available in Appendix B.

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2-7 Watchdog Timer/Power Fail Detector

A watchdog chip (Maxim 690) has been provided to monitor a running program and insure that the processor has not crashed. The watchdog serves several useful functions. First, as the voltage drops below 4.8V, the MAX690 sends out an interrupt (INT4). The interrupt allows stack, flags, and accumulator data to be saved to the battery backed RAM before the system is halted. A program will typically have anywhere from 50-150 ms to perform these "house cleaning" tasks before the reduced power prevents the processor from continuing. The MAX690 will also monitor the SBC's power supply to verify that V_{CC} on the board is stable and above 4.8V DC. The system voltage is compared to the supply and battery voltages. The higher of the two is gated to the SRAM V_{CC} pins to provide constant power to the RAM.

The MAX690 also has a watchdog timer feature. Jumper JP19 (shorted) enables the watchdog. If it is open, the watchdog feature will be disabled. When enabled, the chip select for the 82C55A (at 040h - 043h) is used as a check toggle. The watchdog input must be toggled every 1.6 seconds to insure that the device does not reset. Any access of the 82C55A chip will therefore toggle the watchdog input.

2-8 60-Pin Expansion Header

Included on the MMT-188EB is a 60-pin expansion header for use with add-on peripheral boards. The user has access to all 60 pins by way of a straight PCB header. The following signals are provided via the expansion header:

- ! 20 Address Lines - (BA00 - BA19)
 - " Non buffered processor address lines. Do not drive more than two TTL level loads without external buffering.
- ! 8 Data Lines - (BD00 - BD07)
 - " Non buffered processor data lines. Do not drive more than two TTL level loads without external buffering.
 - " BD08 - BD15 are available at the bus, and are pulled high. However, they are available only to allow compatibility with other MMT products, and are not connected the 80C188EB processor's internal workings.
- ! 2 User Programmable Timers - (TxIN; x=0-1, TxOUT; x=0-1)
 - " Two counter/timers are available to the user to count events or to clock external operations. These counter/timers are directly connected to the 80C188EB's integrated peripheral block. The clock or counting source of both counter/timers can be either external or internal depending on the user's application. For counting purposes input pins TxIN may be used as clock sources.
 - " A third integrated timer is available to the user with only internal clocking available. The timer uses the CPU clock to count events and has no external pins.
- ! Clock Output (CLK)
 - " The CLK output pin operates at 1/2 the CPU's oscillator frequency
- ! Ready Input (READY/WAIT#)
 - " This pin can be used to suspend CPU operation when it is driven low. The normal state of this pin is active high due to an external pull-up resistor.
- ! Offboard Memory Chip Select

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- " The OBMCS# output can be used to address external memory. The memory space assigned to this chip select is user programmable.
- " On units with the 2MB of Flash (U25) installed, the Offboard Memory Chip Select will not be available for the user.
- ! I/O Chip Selects (IO_USER0# - 2#)
 - " These chip selects are driven low during I/O read and write cycles. The I/O space of these chip selects is user programmable. Midwest Micro-Tek has placed them as follows:
 - IO_USER0# 0080h - 00BFh
 - IO_USER1# 00C0h - 00FFh
 - IO_USER2# 0100h - 013Fh
- ! 2 Hardware Interrupt Sources (INT0, INT2)
 - " Active HIGH, pulled down hardware interrupt sources.
- ! Nonmaskable Interrupt (NMI)
 - " The NMI input can be used to interrupt the CPU at any time. When driven high, this signal will cause an interrupt to be generated in the 80C188EB. The NMI pin can be used to exit the 80C188EB from either of its power down modes (Idle and Powerdown).
- ! Reset (RESET)
 - " The RESET line may be used to notify external peripherals that a system reset has occurred. This output is driven high on a system reset.
- ! Hold and Hold Acknowledge (HOLD, HLDA)
 - " Allow other asynchronous bus masters to gain control of the system bus. When HOLD is driven HIGH, it will complete its current bus activity and then float its control, address, and data lines. HLDA is driven HIGH by the processor to acknowledge the transition to the tri-state condition.
- ! Battery Input/Output Stake (VBAT)
 - " May be used to power external devices from the MMT-188EB's battery, or provides an alternate line to attach an external battery for input purposes.

For complete pinout information please refer to Appendix B.

CHAPTER THREE - Programming Reference

3-1 82C55A Programmable Peripheral Interface - PPI (or compatible)

The 82C55A is a general purpose programmable I/O peripheral with 24 I/O pins which may be programmed in 3 groups of 8 and used in 3 major modes of operation. I

Ports are grouped in three 8 bit ports, A B and C. Ports A and B are programmed to all output or all input. Port C is divided into two. The lower part of Port C (bits 0-3) and the upper (bits 4-7) can be set for either input or output as well.

PORT/MEMORY ADDRESSES	I/O DEVICE AND REGISTER
40h	82C55A - PPI -Port A
41h	82C55A - PPI -Port B
42h	82C55A - PPI -Port C
43h	82C55A - PPI - Control Register

Table 3-1.1: PPI I/O Port Addresses

On reset, all pins are configured as inputs and are in a high impedance state. The modes for Port A and B can be separately defined, while Port C is divided into two portions. All output registers are reset when the mode is changed. Programming the 82C55A is begun by writing a Control Word into the Control Register.

3-2 80C188EB Chip Select Unit

The 80C188EB has 10 on-board chip selects, LCS#, UCS#, and GCS0#-GCS7#. The MMT-188EB uses LCS#, UCS#, and GCS0#-GCS7# for selecting memory and peripheral components. LCS# is used to access RAM socket U4. UCS# is similarly used to access ROM/RAM socket U3. GCS0#, GCS1#, and GCS2# are used as IO_USER0# - 2#. GCS3# is used to select the MAX197 A/D converter. The off-board memory chip select is direct connected to GCS4#. GCS5# selects the 82C55A, and GCS6# selects the 74FCT244 line driver to the 8-pin DIP switch. GCS7# is used to select the MAX 527 D/A converter.

Each chip select has a start and stop register. In addition to the memory ranges selected, these registers establish whether the chip select is active for I/O or memory, the number of wait states, response to the READY pin, enable, and ignore stop address options.

3-3 LAN Circuitry - Optional

Available as an option on the MMT-188EB is a system which provides a means of addressing slave MMT-188EB or MMT-188EBs during LAN operation. An 8-pin dip switch and a 74FCT244 data buffer are used to provide the LAN address of slave units simply by reading the I/O port selected by GCS6#. This configuration provides a method of addressing up to 256 slave SBC's in a single LAN system.

CHAPTER THREE - Programming Reference

3-4 MAXIM - MAX197 12-bit Analog-to-Digital Converter - Optional

Also available on the MMT-188EB, is a multi-range, 12-bit data-aquisition system (DAS) with 8+4 bus interface. The MAX197 uses successive approximation and internal track/hold circuitry to convert an analog signal into a 12-bit digital output.

3-5 MAXIM - MAX527 12-bit Digital-to-Analog Converter - Optional

Another option for the MMT-188EB board is a calibrated quad 12-bit voltage output digital-to-analog converter (DAC). The MAX527 contains four 12-bit DACs. Precision output buffer amplifiers are included on-chip to provide voltage outputs. This device features double-buffered interface logic with a 12-bit input register and a 12-bit DAC register.

APPENDIX A - JUMPER SETTINGS

JUMPER	DEFAULT POSITION, DESCRIPTION
JP1	Used to select type of EEPROM in U21.
JP2	Single Pin, RESIN# signal. Used to access the reset signal.
JP3	2&3, ROM Jumper.
JP4	2&3, RAM Jumper.
JP5	1&2, ROM Jumper.
JP6	OUT, ROM Jumper
JP7	OUT, ROM Jumper.
JP8	OUT, ROM Jumper.
JP9	2&3, RAM Jumper.
JP10	2&3, ROM Jumper.
JP11	1&2, ROM Jumper.
JP12	OUT, ROM Jumper.
JP13	OUT, ROM Jumper.
JP14	1&2, Connects CTS0# to GND ("always on" mode.) 2&3 CTS# is connected to pin 7 of the DB9.
JP15	2&3, RS-232 Interface. 1&2 for RS-485, please see " <i>Networking...</i> " on pages 6-8.
JP16	1&2, Connects CTS1# to GND ("always on" mode). 2&3 CTS# is connected to pin 7 of the DB9.
JP17	2&3, RS-232 Interface. 1&2 for RS-485, please see " <i>Networking...</i> " on pages 6-8.
JP19	OUT, Watchdog timer disabled. IN to enable watchdog.
JP24	2&3, ROM Jumper.
JP25	ON, RS-232 Operation. Grounding bypass for RS-485, see " <i>Networking...</i> " on pages 6-8. Channel 0
JP26	RS-485 Mode Jumper. Please see " <i>Networking...</i> " on pages 6-8.
JP27	RS-485 Mode Jumper. Please see " <i>Networking...</i> " on pages 6-8.
JP28	RS-485 Mode Jumper. Please see " <i>Networking...</i> " on pages 6-8.
JP29	RS-485 Mode Jumper. Please see " <i>Networking...</i> " on pages 6-8.
JP30	RS-485 Mode Jumper. Please see " <i>Networking...</i> " on pages 6-8.
JP31	RS-485 Mode Jumper. Please see " <i>Networking...</i> " on pages 6-8.

APPENDIX A - JUMPER SETTINGS

JP37	ON, RS-232 Operation. Grounding bypass for RS-485, see " <i>Networking...</i> " on pages 6-8. Channel 1
JP39	2&3, Enables battery backed RAM
JP43	1&2, Selects PB5 to check if the A/D is finished with a conversion. 2&3 Selects INT2
JP44	Off, Selects the internal 4.096V reference for the A/D, ON use the external reference.

Table A-1: Jumper Defaults and Definitions.

APPENDIX B - PINOUTS, PORT I/O, & MEMORY ASSIGNMENTS

B-1 RS-232 Pinouts

The MMT-188EB RS-232 pinouts are compatible with the IBM PC as DCE equipment. In normal operation, no null modem connector should be needed. With some older terminal equipment, a null connection may be required.

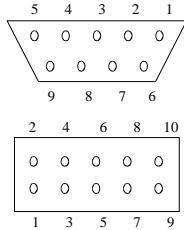


Figure B-1.1: RS-232 Pinouts

10 Pin Stake		DB9 Connector	
Pin	Signal	Pin	Signal
1	NC	1	NC
2	DTR (DSR)	6	DTR (DSR)
3	TxD Input	2	TxD Input
4	CTS Input	7	CTS Input
5	RxD Output	3	RxD Output
6	RTS Input	8	RTS Input
7	DSR (DTR)	4	DSR (DTR)
8	NC	9	NC
9	GND	5	GND
10	NC		

Table B-1.1: RS-232 Pinout

B-2 RS-485 Pinouts

Only 2 pins of the DB9 socket connector are specifically defined for the RS-485 option, these being the Differential + and Differential - pins. No jumpers need to be installed or removed to operate via the RS-485 interfaces (as far as the 10-pin stake is concerned). However, the user must toggle the data direction lines running to the 75176's. These lines are labeled RTS0# and RTS1# on the serial I/O schematics.

10 Pin Stake		DB9 Connector	
Pin	Signal	Pin	Signal
1	DIF+	1	DIF+
8	DIF-	9	DIF-
9	GND	5	GND
2,3,4,5,6,7,10	NC	2,3,4,6,7,8	NC

Table B-2.1: RS-485 Pinouts

APPENDIX B - PINOUTS, PORT I/O, & MEMORY ASSIGNMENTS

B-3 60-Pin Expansion Header

Refer to Section 2-9 for more detailed pin descriptions.

60-Pin Expansion Header			
PIN	I/O SIGNAL	PIN	I/O SIGNAL
1	Ground - GND	2	V _{CC} - +5V DC
3	HLDA - Hold Acknowledge	4	READY# - CPU Ready Line
5	HOLD - CPU Hold	6	IO_USER1# - I/O User Chip Select 1
7	IO_USER0# - I/O User Chip Select 0	8	IO_USER2# - I/O User Chip Select 2
9	OBMCS# - Offboard Memory Chip Select	10	CLK - CPU Clock Signal
11	Data Line 00	12	Address Line 00
13	Data Line 01	14	Address Line 01
15	Data Line 02	16	Address Line 02
17	Data Line 03	18	Address Line 03
19	Data Line 04	20	Address Line 04
21	Data Line 05	22	Address Line 05
23	Data Line 06	24	Address Line 06
25	Data Line 07	26	Address Line 07
27	Data Line 08	28	Address Line 08
29	Data Line 09	30	Address Line 09
31	Data Line 10	32	Address Line 10
33	Data Line 11	34	Address Line 11
35	Data Line 12	36	Address Line 12
37	Data Line 13	38	Address Line 13
39	Data Line 14	40	Address Line 14
41	Data Line 15	42	Address Line 15
43	RD# - Read Line	44	Address Line 16
45	WR# - Write Line	46	Address Line 17
47	INT2 - Hardware Interrupt 1	48	Address Line 18
49	VBAT - Battery Input	50	Address Line 19
51	V _{CC} - +5 V DC	52	Ground
53	T0IN - Timer 0 Input	54	INT0 - Hardware Interrupt 0
55	T1IN - Timer 1 Input	56	RESET - Reset Output
57	T0OUT - Timer 0 Output	58	No Connection
59	T1OUT - Timer 1 Output	60	NMI - Non-Maskable Interrupt

Table B-3.1: 60 Pin Expansion Header Pinout

APPENDIX B - PINOUTS, PORT I/O, & MEMORY ASSIGNMENTS

B-4 OPTO22 Interface

OPTO22 Standard Interface		
PIN	SIGNAL	INPUT (I) OR OUTPUT (O)
1	8255A- PORTA BIT 0	I/O
3	8255A- PORTA BIT 1	I/O
5	8255A- PORTA BIT 2	I/O
7	8255A- PORTA BIT 3	I/O
9	8255A- PORTA BIT 4	I/O
11	8255A- PORTA BIT 5	I/O
13	8255A- PORTA BIT 6	I/O
15	8255A- PORTA BIT 7	I/O
17	8255A- PORTB BIT 0	I/O
19	8255A- PORTB BIT 1	I/O
21	8255A- PORTB BIT 2	I/O
23	8255A- PORTB BIT 3	I/O
25	8255A- PORTB BIT 4	I/O
27	8255A- PORTB BIT 5	I/O
29	8255A- PORTB BIT 6	I/O
31	8255A- PORTB BIT 7	I/O
33	8255A- PORTC BIT 0	I/O
35	8255A- PORTC BIT 1	I/O
37	8255A- PORTC BIT 2	I/O
39	8255A- PORTC BIT 3	I/O
41	8255A- PORTC BIT 4	I/O
43	8255A- PORTC BIT 5	I/O
45	8255A- PORTC BIT 6	I/O
47	8255A- PORTC BIT 7	I/O
49	VCC - +5 Volts	VCC
2-50 (Even)	GND - Ground	Ground

Table B-4.1: OPTO22 Standard Interface - Pinout

APPENDIX B - PINOUTS, PORT I/O, & MEMORY ASSIGNMENTS

B-5 Port/Memory Addresses for the MMT-188EB

PORT/MEMORY ADDRESSES	I/O DEVICE OR MEMORY BLOCK
000h	74FCT244 Chip Select
040h	82C55A - Port A
041h	82C55A - Port B
042h	82C55A - Port C
043h	82C55A - Control Register
080h	IO_USER0
0C0h	IO_USER1
100h	IO_USER2
140h	A/D Converter - MAX197
180h	D/A Converter - MAX527
18Ch	74FCT374 - Paging Flash and control LED's
00000h	Memory Socket U4 (RAM Socket)
70000h	2MB Flash / Off Board Memory Chip Select
80000h	Memory Socket U3 (ROM Socket)

Table B-5.1: Default Port/Memory Assignments