MMT-PIC44

17C44 Microprocessor Board
Rev. F
HARDWARE / SOFTWARE
USER'S REFERENCE MANUAL

MIDWEST MICRO-TEK

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PREFACE

User Feedback

At Midwest Micro-Tek we are always interested in user comments and suggestions. We would like to know how well you like our products. We also like to know if you feel there is something missing either in terms of features offered, or in our documentation. We value your ideas and information!

Customization

Midwest Micro-Tek will modify hardware and software to customer specifications with a minimum quantity purchase, or on a consulting basis.

PRIOR TO INSTALLATION

- **!** Set the necessary jumpers on the MMT-PIC44 board for the memory and I/O configuration intended. See Section 2-5, Memory Configuration on pages 7-13.

- **!** Verify that the terminal cable you are using is correct as specified in Appendix B of this manual. It may be necessary to jumper the CTS (clear to send) signal on the board for communication with your terminal device. The MMT-PIC44 is configured as a DCE device and may require a NULL modem connector to communicate with older PC's. Please check your PC specifications for RS-232 compatibility.

- **!** Midwest Micro-Tek cannot assume responsibility for problems caused by improper power supply connections.

- **!** Before operating the MMT-PIC44 embedded controller, please verify that the +5 volt power supply is plugged into a wall socket, and the power lead is connected to the controller's power jack

PREFACE

Supplemental Materials

This manual provides general information, installation, programming information, principles of operation, and service information for the MMT-PIC44 microcomputer board. Supplemental information may be found in the data sheets included on the CD-ROM. The following data sheets are included on the CD-ROM:

!	**PIC17C44.PDF**	**PIC17C44 Microcontroller Users Manual**
!	**82C55.PDF**	**Programmable Peripheral Interface**
!	**8251A.PDF**	**Programmable Communication Interface**
!	**82C54.PDF**	**Programmable Interval Timer**
!	**93C46.PDF**	**Microchip Serial EEPROM**
!	**MAX197.PDF**	**Maxim 12-Bit A/D Converter**
!	**MAX526.PDF**	**Maxim 12-Bit D/A Converter**
!	**RTC72421.PDF**	**Epson Real Time Clock Users Manual**

The above listed documents make an excellent starting point for learning to program the MMT-PIC44 Microcomputer Board, however, it is beyond the scope of this document to instruct the user in assembly language or high level language programming. For information in these areas the user is referred to the numerous books available on the subject.

User Assistance

If the information you need for configuring this board is not present in this document, please do not hesitate to call us for technical support. At Midwest Micro-Tek, we want to make the use of this board as pleasant and trouble free as possible.

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CHAPTER ONE - SPECIFICATIONS

1-1 Introduction

Thank you for purchasing the MMT-PIC44. We hope that you will find it to be reliable, flexible and easy to use. This board is a complete microcomputer requiring only a +5 volt power supply to operate.

This board has received a 50 hour dynamic burn-in under continuous loop diagnostics to insure a high level of reliability for your product.

Manual Notation

Every discussion of microprocessor systems requires a method of denoting an active low signal. This manual uses a "#" pound symbol following the label name to indicate such signals. Additionally, when referring to bits within a byte, the 8 bits are assumed to be numbered 0 through 7 with 0 being the least significant of these. Lastly, the Designation of "HIGH" and logic level "1" is equivalent to a bit being set and "LOW" or "0" as a bit being cleared is used throughout. All notations used in this manual are consistent with the notations used by major IC industry sources.

The notation used in the jumper tables in this document are as follows:

1&2	A 3-pin block with a jumper installed on pins 1 and 2
2&3	A 3-pin block with a jumper installed on pins 2 and 3
ON	A 2-pin block with a jumper installed
OUT	No jumper installed on this block
XXX	Don't Care

1-2 General Description

Standard Features

- Microchip PIC17C44 CPU at 20MHz (standard)
- Up to 64kx16 bytes of addressable memory
- 2 Serial I/O ports (RS-232 standard or RS-485 optional)
- 39 bits of parallel I/O
- 16-pin header for the special purpose I/O port pins
- 60-pin header for direct access to MCU and peripheral lines

Options

- Clock Calendar IC/Battery Backup
- RS-485 Line Driver/Receiver Option for Serial Communications
- 8-pin DIP switch for LAN Operation
- EPROM, FLASH, serial EEPROM & SRAM
- Parallel, Serial, and Power Cabling
- 8 channels of 12-bit A/D, 4 channels of 12-bit D/A

1-3 Equipment Supplied

- MMT-PIC44 Microcomputer Controller Board
- CD-ROM containing :
  - I/O Equates
  - Sample Code of assembly drivers
  - Manual
  - Data sheets

- " Schematics
- " Silkscreen

1-4 Equipment Required

- ! Serial I/O terminal or PC with communication software (Procomm is suggested)
- ! +5 volt or optionally +9 to +18 volt power supply (650 mA)

1-5 Specification

Standard Features

- ! Intel PIC17C44 microprocessor
  - " 20MHz clock rate for performance (25MHz on request)
  - " Temperature Range - 0 to 70C
- ! 4 RAM/ EPROM/ FLASH sockets
  - " 32 / 28 pin byte wide JEDEC sockets
  - " Possible 64kx16 Kbytes of memory
- ! MCU Onboard Serial I/O port
  - " Software programmable baud rates
  - " Asynchronous rates from 1.2k to 312.5k
  - " RS-232 or RS-485 interface compatible
    - Party line or point-to-point RS-485 interface
    - Communications distances up to 5000 feet
- ! Serial I/O port -(8251 USART controlled)
  - " RS-232 or RS-485 interface
    - Party line or point-to-point RS-485 interface
  - " Asynchronous rate from DC to 300K baud
  - " Synchronous rate from DC to 300K baud
- ! Watchdog Timer
- ! 24 bits of parallel I/O
  - " 24 bits of parallel I/O via Intel 82C55A (or compatible)
    - Terminated to an OPTO22 Standard 50-pin straight header
- ! 60-pin Expansion Header
  - " Access to all address and data lines
  - " 2 timer/counter
  - " Clock output
  - " Memory and I/O read/write lines
  - " Ground and +5 optionally -5 and +12
  - " Reset line
  - " 2 user chip select lines
  - " 2 Maskable interrupt
- ! Onboard timer and Special Function Port Header

Options

- ! Battery Backup for RAM sockets and clock
- ! Clock/Calendar IC
- ! Monitor/Debugger EPROM and 8kx16 SRAM
- ! EPROMS and SRAM

- Power Fail Detector
- Small C
- A/D, D/A

2-1 Installation Considerations

The MMT-PIC44 microcomputer is designed as a stand-alone single board computer (SBC). A Monitor/Debugger EPROM and 8kx16 SRAM are available as an option to allow the user to start exercising the board immediately.

The MMT-PIC44 is shipped without memory devices installed in the 28-pin "byte wide" sockets. However, an 32kx16 Monitor /Debugger EPROM and 32kx16 SRAM can be optionally installed.

2-2 Static Electricity (ESD) Considerations

Memory devices are extremely susceptible to static electricity. When installing memory devices, be sure that the power to the board is off and that pin 1 of the device is properly oriented. A grounded static-dissipating wrist strap should also be used if at all possible in order to minimize possible static damage.

2-3 Jumper Installation

The MMT-PIC44 CPU board has been designed to be extremely flexible in allowing the user to configure memory and I/O as needed for his/ her particular product needs. The following jumper table shows the jumper configuration used at the time of shipment and the function of each of these jumpers.

As shipped the board has jumpers installed for the following configuration.

Jumper	Pin Jumped	Usage
JP20, JP23	ON	By pass both of the 100 ohm serial grounding resisters
JP12	1&2	Ground UART Serial port CTS line
JP14	2&3	Select RS-232 for on board Serial port
JP15	2&3	Select RS-232 for UART Serial port
JP3	1&2	32kx8 EPROM installed in U3
JP8	2&3	32kx8 EPROM installed in U3
JP9	1&2	32kx8 EPROM installed in U5
JP65	1&2	32kx8 EPROM installed in U5
JP10	1&2	32x8 EPROM installed in U5
JP1	2&3	32kx8 RAM installed in U7
JP44	2&3	32kx8 RAM installed in U8

Additional detailed sections are provided describing each of these options.
Refer to Section 2-5: Memory Configuration and Appendix A - Jumper Settings.

2-4 Serial I/O

The 2 DTE type serial interfaces of the MMT-PIC44 board are configured as 9 pin serial interface connectors compatible in pin numbering with the IBM PC 9 pin serial I/O connectors. Both serial

connectors are presented to the outside world via two 10-pin headers, which can be transformed into DB9 socket connectors by way of ribbon cables. Please refer to Appendix B for Proper pinouts of the 10-pin stake headers. The two serial ports can be configured to use either RS-232 and RS-485. Port 2 has CTS and RTS capabilities.

The first serial port is provided through the PIC17C44 Serial (J1, port1) Port lines. This port will send and receive as fast as the MPU timer is capable (312.5K baud). Serial port1 is software programmed.

Also included on the MMT-PIC44 board is an RS-232 or RS-485 interface that operates via an 8251A USART programmable communication interface (J2, port2) . This interface can operate at up to 300k baud.

The RS-232 is the 'standard' interface used by most computer users and will be the interface of choice for most users. Cabling distances of up to 50 feet are possible at 9600 baud, with longer distances possible as the baud rate is decreased. The RS-485 interface selection is capable of operating reliably at separation distances of up to 5000 feet.

Refer to Appendix B for Serial I/O connector pinouts.

The jumpers JP14 and JP15 are used to select the RS-232 or RS-485 serial I/O interface for serial ports 1 and 2. Refer to Appendix A for jumper configuration.

JP17 and JP11 should almost always be shorted. They should only be left open if a static charge builds up during RS-485 operation.

RTS and CTS Considerations

The RTS# port 2 control signal has two basic functions. When using the RS-232 interface, RTS# is used as handshaking signal to drive pin 8 of the DB9 socket connectors. During RS-485 operation, RTS# is used to control whether the 75176 Line Driver IC is transmitting or receiving. When RTS# is cleared, the 75176 receives data from the serial port. When this bit is set, the 75176 transmits data out the serial port. The 75176 device for port 1 is controlled by a bit on the 74373 and it's operation is detailed in the Serial Peripheral section.

Note: When using the RS-232 or RS-485 interface, the RTS# and '373 lines are not automatically toggled. The user must manually set or reset these signals.

The CTS# input on the 82C51 is used as a handshaking signals to control the data flow on the serial I/O channels. When CTS# is tied directly to ground, the serial channel is in "receive always" mode.

The CTS# signal can be tied directly to ground (default setting) with jumpers JP12, or sent out to the DB9 socket connections to be driven by other I/O devices.

RS-485 Operation:
RS-485 interface usage allows the separation of MMT-PIC44 and peripheral up to 5000 feet. A

75176 IC is used to accomplish this thru the use of a differential pair. Please note that full duplex configuration is not possible and that the device desiring to transmit must raise the direction control line of the 75176. (The 74373 S0_485T line is used to toggle the port1's 75176. The UART uses the RTS# line to toggle it's 75176 As a result, a Master/Slave relationship under software control is generally the most straight forward communications scheme to implement.)

Networking using RS-485
Various RS-485 configurations:

1. Interfacing one SBC to a PC using a serial link:

! To use only one SBC interfaced to a PC, one needs to set up the SBC using the 75176 setup on the far left of Figure 2-4.1. In doing so, enable the 100 ohm and both the 560 (or 1K) ohm resistors. Next determine if both the PC and SBC are connected to a common earth ground. If this is not the case, enable the 100 ohm resistor and add a grounding wire to your twisted pair. The 100 ohm resistor insures that a damaging current build up between the two ports is prevented. Refer to tables 2-4.1 and 2-4.2 for the biasing and grounding jumper settings.

2. Interfacing two SBC's together:

! To interface two SBC's, refer to the two outer 75176 configurations on Figure 2-4.1. Configure the first (master) board as described in Part 1 of this page and configure the second (slave) board by enabling the 100 ohm biasing resistor. Refer to tables 2-4.1 and 2-4.2 for the biasing and grounding jumper settings. Again, if a common ground is not present, enable the grounding resistor on each board and add a grounding wire to the twisted pair.

3. Interfacing more than two SBC's:

! When interfacing more than two SBC's, refer to the entire Figure 2-4.1. As shown, as many as 32 nodes can be added in line with the twisted pair. Note that any board that is added to the network should not have any of the biasing resistors enabled since the master board is performing the biasing for the entire network. The only boards that need the biasing resistors enabled is the master (first terminal node) and the last board (final terminal node). Refer to tables 2-4.1 and 2-4.2 for the biasing and grounding jumper settings. If one or two or any number of the boards do not share a common earth ground, one must enable the grounding resistor and add a grounding wire to the twisted pair.

Configuration	JP14	JP21	JP18	JP20	JP17
Master	1&2	ON	ON	ON	*
Final Node	1&2	ON	OUT	OUT	*
Additional Nodes	1&2	OUT	OUT	OUT	*
RS-232 Operation	2&3	XXX	XXX	XXX	ON

Table 2-4.1: Channel 1 biasing and grounding jumper table

Configuration	JP15	JP19	JP23	JP22	JP11
Master	1&2	ON	ON	ON	*
Final Node	1&2	ON	OUT	OUT	*
Additional Nodes	1&2	OUT	OUT	OUT	*
RS-232 Operation	2&3	XXX	XXX	XXX	ON

Table 2-4.2: Channel 2 biasing and grounding jumper table

* This is the grounding resistor jumper. To enable it, **DO NOT** place a jumper on the block. To disable it, place a shorting jumper on the block. Refer to instructions on in this section for use. (Please note that a jumper must ALWAYS be placed on this block when in the RS-232 mode.

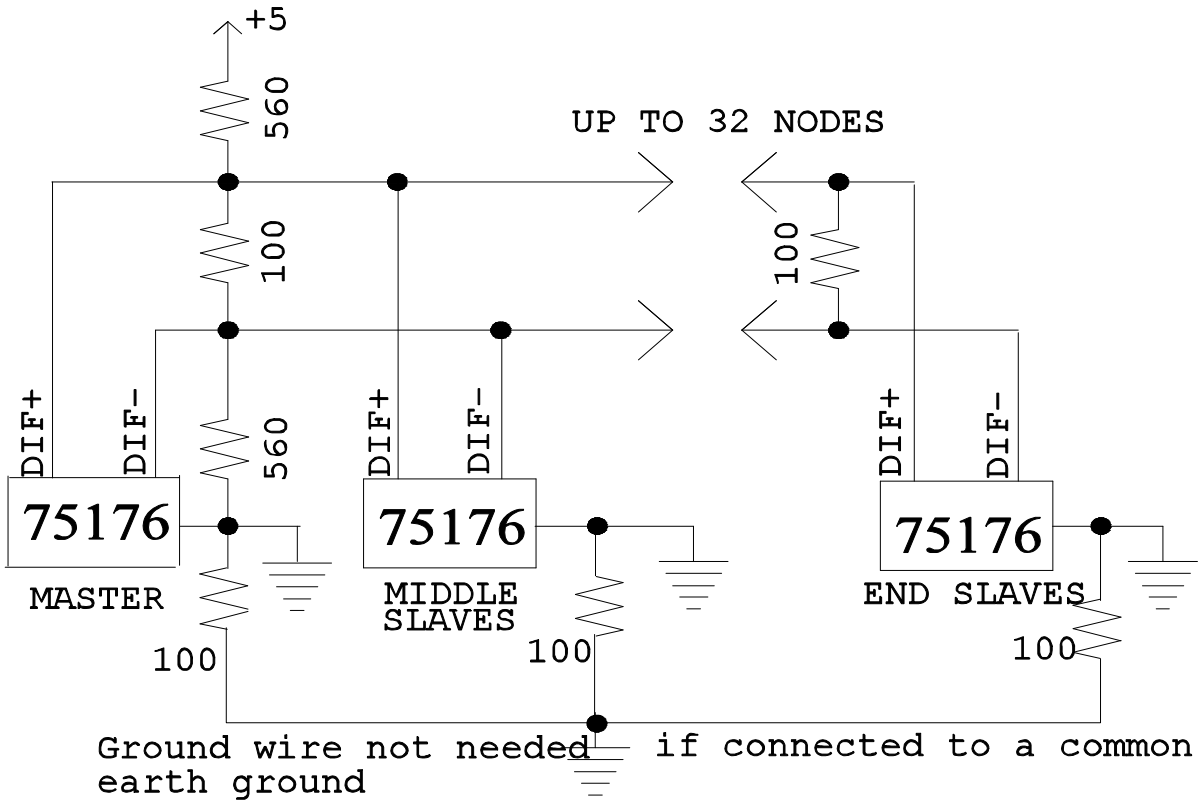


Figure 2-4.1: RS-422/485 Network Schematic

2.5 Memory Configuration

The 'byte-wide' sockets of the MMT-PIC44 board have been configured to be as flexible as possible within cost and board real estate considerations. As a result, only a certain variety of chip types and sizes may occupy each socket. The following list outlines the types of memory supported:

U3 -ROM
EPROM 8kx8, 16kx8, or 32kx8 type devices.
FLASH 32kx8 type devices.

U5 - ROM
EPROM 8kx8, 16kx8, or 32kx8 type device
FLASH 32kx8 type devices

U7 and U8 - RAM
8kx8 or 32kx8 RAM devices

JUMPER CHIP TYPE	JP2	JP3	JP8	JP6
8kx8 EPROM	XXX	1&2	2&3	XXX
16kx8 EPROM	XXX	1&2	2&3	XXX
32kx8 EPROM	XXX	1&2	1&2	XXX
32kx8 FLASH	2&3	XXX	1&2	IN FOR 12 VOLT

Table 2-5.1 - Memory Socket U3 Jumper Configuration (ROM OR FLASH)

JUMPER	U7 8kx8 SRAM	U7 32kx8 SRAM	U8 8kx8 SRAM	U8 32kx8 SRAM
JP1	2&3	1&2	XXX	XXX
JP44	XXX	XXX	2&3	1&2

Table 2-5.2 - Memory Socket U7 and U8 Jumper Configuration (RAM)

JUMPER	JP9	JP10	JP65	JP7	JP69	JP70	JP71	JP72
8kx8 EPR0M	1&2	1&2	1&2	XXX	XXX	XXX	XXX	XXX
16kx8 EPROM	1&2	1&2	1&2	XXX	XXX	XXX	XXX	1&2
32kx8 EPROM	1&2	2&3	1&2	XXX	XXX	XXX	2&3	1&2
32kx8 FLASH	XXX	2&3	XXX	in for +12V	2&3	2&3	2&3	1&2

TABLE 2-5.3 Memory Socket U5 Jumper Configuration

2-6 Parallel Port

The MMT-PIC44 makes use of the Intel 82C55A (or compatible) programmable peripheral interface to provide 24 lines of parallel I/O between the user's peripheral devices and the PIC17C44 data bus. The 82C55A divides these 24 lines into three ports (A, B, and C) of eight lines each. In addition, port C is divided into two groups of four lines each. The 82C55A is software programmable for three modes of operation. Each mode can be configured for various types of I/O formats.

The MMT-PIC44's parallel I/O is terminated into an OPTO22 compatible 50-pin header. Note: A relay in NOT provided to control the state of pin 49 of the OPTO header. Instead, pin 49 is used to supply +5 V to the 50-pin header.

The 82C55A resides in I/O space and is selected through 8255_CS# at the following address:

OPTO22 - 1 8255_CS# FF00h - FF03h

Header pinouts are available in Appendix B.

The 82C55A can also control an LCD with a standard 14 pin (16 with LED backlit) sip header. The low nibble of port A controls the data (note: the header configuration is for a 4 bit bus) bus. Bit 4 of port A controls the Enable line and Bit 5 of port A controls the R/S line. J8 is a 16 pin header located next to the memory chips and pin one is marked with an *. It's pin out is as follows

Pin1 Ground
Pin2 +5
Pin3 Vee adjust (pot resister R28 adjust Vee or display intensity)
Pin4 R/S line
Pin5 R/W line (not used, grounded for always write)
Pin6 Enable line
Pin7 data line 0 (not used, grounded)
Pin8 data line 1 (not used, grounded)
Pin9 data line 2 (not used, grounded)
Pin10 data line 3 (not used, grounded)
Pin11 data line 4 (connected to port A Bit 0)
Pin12 data line 5 (connected to port A Bit 1)
Pin13 data line 6 (connected to port A Bit 2)
Pin14 data line 7 (connected to port A Bit 3)
Pin15 grounded (used by LED backlit displays)
Pin16 +5 (used by LED backlit displays)

A 4x4 matrix keypad is also supported by the 82C55. Connection is made at J9, pin 1 is * and is connected as follows

Pin1 - Port A Bit 0
Pin2 - Port A Bit 1
Pin3 - Port A Bit 2
Pin4 - Port A Bit 3
Pin5 - Port B Bit 4 (Note: this line pulled low)
Pin6 - Port B Bit 5 (Note: this line pulled low)
Pin7 - Port B Bit 6 (Note: this line pulled low)
Pin8 - Port B Bit 7 (Note: this line pulled low)

2-7 Expansion Bus

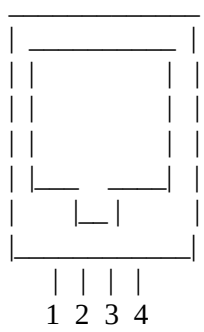
Included on the MMT-PIC44 is a 60 pin expansion header, EXPA1, for use with add-on peripheral boards (pin1 is *). The user has access to all 60 pins by way of a straight IDC header. The following signals are provided via the expansion header:

- 20 Address Lines - (BA00 - BA19)
  - Buffered processor address lines.
- 16 Data Lines - (BD00 - BD15)
  - Non buffered processor data lines. Do not drive more than two TTL level loads without external buffering.
- 2 User Programmable Timers - (T0IN, T1IN, T0OUT, T1OUT, T0GATE, T1GATE)
  - Two counter/timers are available to the user to count events or to clock external operations. They can be configured for various clock speeds by way of the Intel 8254. The user can supply the input clock (T0IN and T1IN) for the timer of jumpers JP24 and JP25 can be used to supply the 8MHz peripheral clock to the timer. The gate pins are pulled high but are available to the user.
- Clock Output (CLK)
  - The CLK output pin operates at 8MHz (peripheral oscillation frequency)
- I/O Chip Selects (IO_USER1#, IO_USESR2#)
  - These chip selects are driven low during I/O read and write cycles. The I/O space of these chip selects is user programmable. Midwest Micro-Tek has placed them as follows:
    - IO_USER1# FFC0h - FFDFh
    - IO_USER2# FFE0h - FFFFh
- Hardware Interrupt Source (INT0)
  - Programable active LOW or active HIGH, it is inverted to comply with other MMT products.
- Hardware Interrupt Source (INT1) (TOCKI input)
  - Like INT0, INT1 is programable active HIGH or LOW and is also inverted to comply with other MMT products.
- Reset and Reset# (RESET, RESET#)
  - The RESET and RESET# lines may be used to notify external peripherals that a system reset has occurred. RESET is driven high and RESET# is driven low on a system reset.
- System processor lines (WR#, RD#, ALE, +12, +5, GND, -5)

For complete pinout information please refer to Appendix B.

2 - 8 I2C bus

An I2C bus is provided on the MMT-PIC44 board. J4 is an RJ-11 jack and is wired in accordance with ACCESS(TM) bus specifications. The board can use the I2C bus but must bit-bang the information, examples of bit-banging can be found on your includes disk. The output of the RJ-11 jack is shown below.



Pin1 - GND
Pin2 - SDA
Pin3 - +5V
Pin4 - SCL

2 - 9 Dip Switch

The 7 position dip switch can be accessed by reading I/O location FF14. If a switch position is "ON" then the corresponding Bit will be set. Bit 7 of I/O location FF14 is used to receive serial information from the various serial peripherals

2 - 10 The Intel 8254 Counter/Timer

An Intel 8254 Counter/Timer is available at I/O location FF20. Timer 2 is used by the 8251 serial port but timers zero and one can be used by the user. The user can supply a clock at the timer input pins or the 8MHz peripheral clock can be sent to the input via jumpers JP24 and JP25. JP24 provides the 8MHz clock to timer 1 and JP25 provides the 8MHz clock to timer 2. Examples of how to use these clocks can be found on you includes disk. One should have access to an Intel peripheral components hand book, or the data sheets can be down loaded from the Intel web page.

2 - 11 The Intel 8251 serial chip

A second serial port is provided by the Intel 8251 serial chip. Timer 2 of the Intel 8254 counter/timer provides the clock input for both the input and output. The TXD, RXD, CTS, and RTS lines are brought out to the 10 pin stake header J2 (see appendix A for pinouts). As with the 8254 counter/timer, the user should have access to an Intel peripherals handbook or the data sheets can be down loaded on the Intel web sight. Examples of how to initialize and utilize this serial port can be found on the includes disk.

2 - 12 The EPSON Real Time Clock (RTC)

The RTC can be run off the battery backup supply or it can be connected directly to the on board +5V power supply via JP63. Set to the 1&2 position and the clock runs off +5V, the 2&3 position will provide the clock with battery backed power. The RTC can send an interrupt to the processor though either the INT0 or INT1 interrupts. Setting JP62 to the 1&2 position will send the interrupt to INT1 and setting the 2&3 position will send the interrupt to INT0. For programming and operating examples see the includes disk and see the attached RTC data sheets found at the end of this manual.

2 - 13 The Serial Peripherals

This serial port can emulate an SPI port All the serial peripherals are controlled by a 74LS373 (U22) located at I/O address FF14h. Before discussing the serial devices and how they are accessed it should be noted that Bits 2, 3, 4, 5, and 7 have uses other than controlling the serial peripherals. The following table shows the usage of the 8 I/O Bits.

BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
Serial Datain	Serial Clock	NOT USED	serial port 1 RS485 Control	status LED control	status LED control	Serial EPROM chip select	status LED control

Bit 3 is used to toggle the Send/Receive pin on the 75176(RS-485) chip for onboard serial port. To receive set Bit 3 to 1, to send clear the Bit to 0.

Bit 7 controls status LED D5. Bit 4 controls LED D1. Bit 5 controls LED D2. Setting the Bits will turn the LED on and clearing them will shut them off.

NOTE: Since this I/O register is a WRITE ONLY register the MCU cannot determine the state of the register. It is a good idea to write the contents to a ram location at the same time the register is written to. When the programmer needs to know what is at the register location it can easily be read from the shadow ram location.

The serial EEPROM is controlled by the 74LS373. This device requires 4 control lines consisting of a chip select line, data in line, data out line, and a clock. This port can simulate an SPI port. There are many example on how to use the serial device on the includes disk and it is quite easy to use the routines in other programs. Data sheets for the serial EEPROM can be down loaded from the Microchip BBS or from there WEB site. To send to and receive data from a serial device follow the steps below.

1. Select the device. Setting Bit 6 will select the serial EPROM

2a. To send data, write the LSB to Bit 0 then set and clear Bit 1.

2b. To receive data, set and clear Bit 1 then read the data present at I/O location FF80h. Bit 7 of this location will contain the data bit being sent by the serial device.

3. After all the information has been sent and received, deselect the device.

Remember that examples of reading and writing all of the serial devices can be found on the includes disk. Study these examples and the data sheets carefully before attempting to use the serial devices.

! The Serial EEPROM

Midwest Micro-Tek provides a 93C46 EEPROM at U29, however any 4 line EEPROM can be used. The Microchip 93C46 is an 8 or 16 bit device whose data width can be selected at jumper JP16. Set the jumper to the 1&2 position for 8 bits and set to 2&3 for 16 bits.

CHAPTER THREE - PROGRAMMING REFERENCE

3-1 82C55A Programmable Peripheral Interface - PPI (or compatible)

The 82C55A is a general purpose programmable I/O peripheral with 24 I/O pins which may be programmed in 2 groups of 12 and used in 3 major modes of operation. In Mode 0, each group of 12 I/O pins may be programmed in sets of 4 for input or output. Mode 1 allows each group to have 8 lines of input or output, of the remaining 4 pins, 3 are used for handshaking signals. Mode 2 is the bidirectional bus mode with 8 lines for a bidirectional bus, and 5 lines borrowing one from the other group for handshaking.

The majority of embedded applications make use of Mode 0 which fully utilizes the 82C55A's I/O lines and allows easy implementation of switching logic.

Ports are grouped in 12 bit lots with Port A and Port C Upper (C7 - C4) making up one group, and Port B and Port C Lower (C3 - C0) making up the other.

PORT/MEMORY ADDRESSES	I/O DEVICE AND REGISTER
FF00h	82C55A - PPI -Port A, Unit A
FF01h	82C55A - PPI -Port B, Unit A
FF02h	82C55A - PPI -Port C, Unit A
FF03h	82C55A - PPI - Control Register. Unit A

Table 3-1.1: PPI I/O Port Addresses

On reset, all pins are configured as inputs and are in a high impedance state. The modes for Port A and B can be separately defined, while Port C is divided into two portions. All output registers are reset when the mode is changed. Programming the 82C55A is begun by writing a Control Word into the Control Register.

PPI Mode Set Control Word

- Bit 2,1,0 - Group B Control
  - Bit 0 - Port C Lower
    - XXXXXXX0 - Output
    - XXXXXXX1 - Input
  - Bit 1 - Port B
    - XXXXXX0X - Output
    - XXXXXX1X - Input
  - Bit 2 - Mode Selection
    - XXXXX0XX - Mode 0
    - XXXXX1XX - Mode 1
- Bits 6,5,4,3 - Group A Control
  - Bit 3 - Port C Upper
    - XXXX0XXX - Output
    - XXXX1XXX - Input
  - Bit 4 - Port A

- XXX0XXXX - Output
- XXX1XXXX - Input

" Bit 6,5 - Mode Selection
- X00XXXXX - Mode 0
- X01XXXXX - Mode 1
- X1XXXXXX - Mode 2

! Bit 7 - Mode Set Flag
- 1XXXXXXX - Active
- Set to 1 to indicate that the mode of the PPI is being changed. All outputs are reset, and all inputs are high impedance.

Any of the eight bits of Port C can be set or reset using a single OUTput instruction. A Control Word with Bit 7 set to 1 is considered an Mode Set Command as defined above. A Control Word with Bit 7 set to 0 is considered a Bit Set/Reset Word, and has the following format:

PPI Bit Set/Reset Control Word

! Bit 0 - Bit Set/Reset
" XXXXXXX0 - Reset
" XXXXXXX1 - Set

! Bit 3,2,1 - Bit Select
" XXXX000X - Port C Bit 0
" XXXX001X - Port C Bit 1
" .. etc ..
" XXXX111X - Port C Bit 7

! Bit 6, 5, 4 - Don't Care - Set to 0 for compatibility with future Intel™ products

! Bit 7 - Bit Set/Rest Flag
" 0XXXXXXX - Active

Mode 0 - Basic Input/Output Configurations

! Two 8-bit ports and two 4-bit ports.
! Any port can be input or output.
! Outputs are latched
! Inputs are not latched
! 16 different Input/Output configurations are possible in this mode.

Mode 1 - Strobed Input/Output Configuration

! Two groups (Group A and Group B)
! Each group contains one 8-bit data port and one 4-bit control/data port
! The 8-bit port can be either input or output. Both inputs and outputs are latched
! The 4-bit port is used for control and status of the 8-bit data port.
" Input Control Signal Definition
- Port C Bit 4,2 - $STB_{A,B}$ - Strobe Input. A low on this input loads data into the input latch.
- Port C Bit 5,1 - $IBF_{A,B}$ - Input Buffer Full F/F. A high on this output indicates that the data is loaded in the input latch, an acknowledgment. IBF is set by STB input being low and is reset by a rising edge on the RD# input.

- Port C Bit 3,0 - $INTR_{A,B}$ - Interrupt Request. A high on this output can interrupt the CPU. It is reset by the falling edge of RD#
- Setting Port C Bit 4,2 enables the $INTR_{A,B}$ line if IBF is high.
- Port C Bit 7,6 - May be used as Inputs or Outputs depending upon Bit 3 of the Control Word.

" Output Control Signal Definition

- Port C Bit 6,2 - $ACK\#_{A,B}$ - Acknowledge Input. A low on this input informs the 82C55A that the data from port A or B has been accepted. A response from the peripheral that the data has been transferred.
- Port C Bit 7,1 - $OBF\#_{A,B}$ - Output Buffer Full F/F. The OBF output will go low to indicate that the CPU has written data to the specified port
- Port C Bit 3,0 - $INTR_{A,B}$ - Interrupt Request. A high on this output can interrupt the CPU. It is reset by the falling edge of WR#
- Setting Port C Bit 6,2 enables the $INTR_{A,B}$ OBF is high.
- Port C Bit 5,4 - May be used as Inputs or Outputs depending upon Bit 3 of the Control Word.

Mode 2 - Strobed Bidirectional Bus Input/Output Configuration

! Used in Group A only. (Port B can be used in Mode 1 or 0 simultaneously)
! One 8-bit, bi-directional bus port (Port and a 5-bit control port (Port C)
! Both inputs and outputs are latched
! The 5-bit control port is used for control and status for the 8-bit bi-directional bus port.

" Bidirectional Bus I/O Control Signal Definition

- Port C Bit 6 - $ACK\#_{A}$ - Acknowledge Input. A low on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer is in the high impedance state.
- Port C Bit 7 - $OBF\#_{A}$ - Output Buffer Full F/F. The OBF output will go low to indicate that the CPU has written data to port A.
- Port C Bit 3 - $INTR_{A}$ - Interrupt Request. A high on this output can interrupt the CPU for both input and output operations.
- Setting Port C Bit 6 enables the output interrupts.
- Port C Bit 4 - STB_{A} - Strobe Input. A low on this input loads data into the input latch.
- Port C Bit 5 - IBF_{A} - Input Buffer Full F/F. A high on this output indicates that the data is loaded in the input latch.
- Setting Port C Bit 4 enables the input interrupts.
- Port C Bit 2,1,0 - May be used as Inputs or Outputs depending upon Bit 0 of the Control Word.

Port C may be read in Mode 1 or Mode 2 to allow the programmer to verify the status of each peripheral and branch the code as required. A port read provides the user the following information as defined in Table 3-1.2

Mode 1 Input Configuration							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
MODE 1 OUTPUT CONFIGURATION							
$OBF\#_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$OBF\#_B$	$INTR_B$
MODE 2 STATUS WORD FORMAT							
$OBF\#_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	XXX	XXX	XXX

Table 3-1.2: Port C Status

3-2 I/O Addressing

The MCU parallel data bus is externally available to the user by way of 2 I/O chip selects. These chip selects (IO_USER1 and IO_USER2) are available at the 60-pin expansion bus.

When the port addresses for IO_USER1 and IO_USER2 are written to, the contents of the parallel data bus is reflected at the 60-pin expansion header. These user chip selects can be used to enable peripherals or control other devices such as an A/D converter. The port addresses for each of the user chip selects is as follows:

IO_USER1 - FFC0 to FFDF hex
IO_USER2 - FFE0 to FFFF hex

3-4 LAN Circuitry - Optional

Available as an option on the MMT-PIC44 is a system which provides a means of addressing slave MMT-PIC44s during LAN operation. An 7-pin dip switch and a 74LS244 data buffer are used to provide the LAN address of slave units simply by reading the I/O port at FF80h. This configuration provides a method of addressing up to 128 slave SBC's in a single LAN system.

CHAPTER FOUR - MONITOR/DEBUGGER

4-1 At this time MMT does not have it's own monitor/debugger. However we currently developing one wihich we hope to make available soon..

APPENDIX A - JUMPER SETTINGS

***** (Jumpers JP4, JP36, JP37, JP56, JP57, JP58, JP59, and JP67 serve no function.)**

A-1 Mode Select

Mode	JP53
MCU Mode	1&2
Single Chip Mode	2&3

A-2 Timer Options

	JP25
TIMER0 supplied by 8MHz peripheral clock	ON
TIMER0 supplied by user	OFF

	JP24
TIMER1 supplied by 8MHz peripheral clock	ON
TIMER1 supplied by user	OFF

	JP40
TCLK12 supplied by 8MHz peripheral clock	**ON**
TCLK12 supplied by user	**OFF**

	JP41
TCLK3 supplied by 8MHz peripheral clock	**ON**
TCLK3 supplied by user	**OFF**

A-3 Serial I/O Section

Serial Channel 1 (Onboard Serial Port, J1 on MMT-PIC44)

	JP14
RS-232 Mode	2&3
RS-485 Mode	1&2

Serial Channel 2 (UART, J2 on MMT-PIC44)

	JP12
CTS grounded (always on)	1&2
CTS routed to serial port	2&3

	JP15
RS-232 Mode	2&3
RS-485 Mode	1&2

A-5 I2C Configuration

The SDA (RB6) and SCL(RB7) lines for the I2C bus can be directed to either the RJ-11 jack or they can be sent to the MCU I/O header J3 using JP51 and JP52.

	JP51	JP52
SDA sent to J3	**XXX**	**2&3**
SDA sent to RJ-11	**XXX**	**1&2**
SCL sent to J3	**2&3**	**XXX**
SCL sent to RJ-11	**1&2**	**XXX**

A - 6 A Third Serial Port

A third serial port can be implemented on the MMT-PIC44 by hardwiring pins 1&3 of JP38 and JP39 together. This will send PWM1 and PWM2 out to a RS-232 serial leveler. The serial lines can then be bit-banged to effect a serial port. Examples of how to do this with Microchip devices can be down loaded from the Microchip WEB site.

Pin 1 of J5 is * and has the following pin outs
Pin1 - ground
Pin2 - RXD
Pin3 - TXD

APPENDIX B- PINOUTS, PORT I/O, & MEMORY ASSIGNMENTS

B-1 RS-232 Pinouts

The MMT-PIC44 RS-232 pinouts are compatible with the IBM PC as DCE equipment. In normal operation, no null modem connector should be needed. With some older terminal equipment, a null connection may be required.

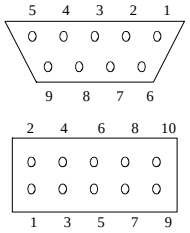


Figure B-1.1: RS-232 Pinouts

10 Pin Stake		DB9 Connector	
Pin	Signal	Pin	Signal
1	NC	1	NC
2	DTR (DSR)	6	DTR (DSR)
3	TxD Input	2	TxD Input
4	CTS Input	7	CTS Input
5	RxD Output	3	RxD Output
6	RTS Input	8	RTS Input
7	DSR (DTR)	4	DSR (DTR)
8	NC	9	NC
9	GND	5	GND
10	NC		

Table B-1.1: RS-232 Pinout

B-2 RS-422 Pinouts

Only 2 pins of the DB9 socket connector are specifically defined for the RS-485 option, these being the Differential + and Differential - pins. The user must toggle the data direction lines running to the 75176's. These lines are labeled RTS0# and RTS1# on the serial I/O schematics. To tie the direction lines RTS0# and RTS1# together, place a shorting jumper on JP17.

The user may wish to disable the other active RS232 lines (CTS and RTS), so that these wires of a party line cable may serve other functions. To do this, remove all jumpers from JP13, JP14, JP15, and JP16.

10 Pin Stake		DB9 Connector	
Pin	Signal	Pin	Signal
1	DIF+	1	DIF+
8	DIF-	9	DIF-
9	GND	5	GND
2,3,4,5,6,7,10	NC	2,3,4,6,7,8	NC

Table B-2.1: RS-422/485 Pinouts

B-3 60-Pin Expansion Header (Pin1 is marked with *)

Refer to Section 2-9 for more detailed pin descriptions.

60-Pin Expansion Header			
PIN	I/O SIGNAL	PIN	I/O SIGNAL
1	Ground - GND	2	V_{CC} - +5V DC
3	NC	4	NC
5	ALE	6	IO_USER1# - I/O User Chip Select 1
7	T0GATE	8	IO_USER2# - I/O User Chip Select 2
9	T1GATE	10	CLK - 8MHz peripheral clock Signal
11	Data Line 00	12	Address Line 00
13	Data Line 01	14	Address Line 01
15	Data Line 02	16	Address Line 02
17	Data Line 03	18	Address Line 03
19	Data Line 04	20	Address Line 04
21	Data Line 05	22	Address Line 05
23	Data Line 06	24	Address Line 06
25	Data Line 07	26	Address Line 07
27	Data Line 08	28	Address Line 08
29	Data Line 09	30	Address Line 09
31	Data Line 10	32	Address Line 10
33	Data Line 11	34	Address Line 11
35	Data Line 12	36	Address Line 12
37	Data Line 13	38	Address Line 13
39	Data Line 14	40	Address Line 14
41	Data Line 15	42	Address Line 15
43	RD# - Read Line	44	Address Line 16
45	WR# - Write Line	46	Address Line 17
47	+12 volts	48	Address Line 18
49	-5 volts	50	Address Line 19
51	V_{CC} - +5 V DC	52	GND - Ground
53	T0IN - Timer 0 Input	54	INT0 - Hardware Interrupt
55	T1IN - Timer 1 Input	56	RESET - Reset Output
57	T0OUT - Timer 0 Output	58	RESET# - inverted Reset Output
59	T1OUT - Timer 1 Output	60	INT1 - Hardware Interrupt

Table B-3.1: 60 Pin Expansion Header Pinout

B-4 OPTO22 Interface (Pin1 is marked with *)

OPTO22 Standard Interface		
PIN	SIGNAL	INPUT (I) OR OUTPUT (O)
1	8255A PORTA BIT 0	I/O
3	8255A PORTA BIT 1	I/O
5	8255A PORTA BIT 2	I/O
7	8255A PORTA BIT 3	I/O
9	8255A PORTA BIT 4	I/O
11	8255A PORTA BIT 5	I/O
13	8255A PORTA BIT 6	I/O
15	8255A PORTA BIT 7	I/O
17	8255A PORTB BIT 0	I/O
19	8255A PORTB BIT 1	I/O
21	8255A PORTB BIT 2	I/O
23	8255A PORTB BIT 3	I/O
25	8255A PORTB BIT 4	I/O
27	8255A PORTB BIT 5	I/O
29	8255A PORTB BIT 6	I/O
31	8255A PORTB BIT 7	I/O
33	8255A PORTC BIT 0	I/O
35	8255A PORTC BIT 1	I/O
37	8255A PORTC BIT 2	I/O
39	8255A PORTC BIT 3	I/O
41	8255A PORTC BIT 4	I/O
43	8255A PORTC BIT 5	I/O
45	8255A PORTC BIT 6	I/O
47	8255A PORTC BIT 7	I/O
49	VCC - +5 Volts	VCC
2-50 (Even)	GND - Ground	Ground

Table B-4.1: OPTO22 Standard Interface - Pinout

B-5 A/D Connector

The A/D connector is located on the upper left hand corner of the MMT-PIC44. It is composed of 10 screw type terminals. Starting from left to right the terminal designation is as follows:

PIN #	A/D PORT
1	GND
2	GND
3 (CH0)	0
4 (CH1)	1
5 (CH2)	2
6 (CH3)	3
7 (CH4)	4
8 (CH5)	5
9(CH6)	6
10(CH7)	7

Table B-5.1: A/D Header

The D/A connector is located behind the A/D connector and is labeled on the silk screen

B-6 MCU I/O Port Expansion Header (Pin1 is marked by the headers label, J3)

Some of the pins available on the 80C51/256 MCU are not necessary to the operation of the SBC but they may be useful to the user. Therefore these pins have been brought out to a 16 pin header (J3) and have been pulled high or low as required for normal operation. Below is a diagram of the pins that have been made available to the user.

PIN	I/O SIGNAL	PIN	I/O SIGNAL
1	CAP1 - Not Pulled	2	TCLK12
3	CAP2 - Not Pulled	4	TCLK3
5	PWM1 - Pulled High	6	NC
7	PWM2 - Not Pulled	8	NC
9	RA2 - Pulled Low	10	GND
11	RA3 - Pulled High	12	GND
13	RB7 - Pulled High	14	GND
15	RB6 - Pulled High	16	GND

Table B-6.1: MCU Port Expansion Header

APPENDIX B- PINOUTS, PORT I/O, & MEMORY ASSIGNMENTS

B-7 Port/Memory Addresses for the MMT-PIC44

PORT/MEMORY ADDRESSES	I/O DEVICE OR MEMORY BLOCK
FF00h	82C55A - Port A
FF01h	82C55A - Port B
FF02h	82C55A - Port C
FF03h	82C55A - Control Register
FF04h-FF05h	LSB/MSB A/D chip selects
FF08h	D/A MSB load
FF0Ch	D/A LSB load
FF10h	D/A latch
FF14	Serial Device Control Register (74LS373)
FF20h	8254A R/W Counter 0
FF21h	8254A R/W Counter 1
FF22h	8254A R/W Counter 2
FF23h	8254A Control Register
FF40h	8251A Data Register
FF41h	8251A Status Register
FF60h-FF6Fh	EPSON RTC registers
FF80h	7 Pin Dip Switch and Serial Device Data Input
FFC0	IO_USER1 Chip Select
FFE0h	IO_USER2 Chip Select

Table B-7.1: Port/Memory Address

APPENDIX B- PINOUTS, PORT I/O, & MEMORY ASSIGNMENTS

B - 8 External Memory Map

FFFF FE00	I/O SPACE
FDFF 8000	SRAM
7FFF 0000	ROM